**FUJITSU SEMICONDUCTOR
DATA SHEET**

DS05-10151-4E

MEMORY

CMOS 512K × 8 BIT
FAST PAGE MODE DYNAMIC RAM

MB81V4800S-60/-70

CMOS 524,288 × 8 bit Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB81V4800S is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 8-bit increments. The MB81V4800S features a "fast page" mode of operation whereby high-speed access of up to 512 × 8-bits of data can be selected in the same row. The MB81V4800S-60/-70 DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB81V4800S is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to +4.6	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.
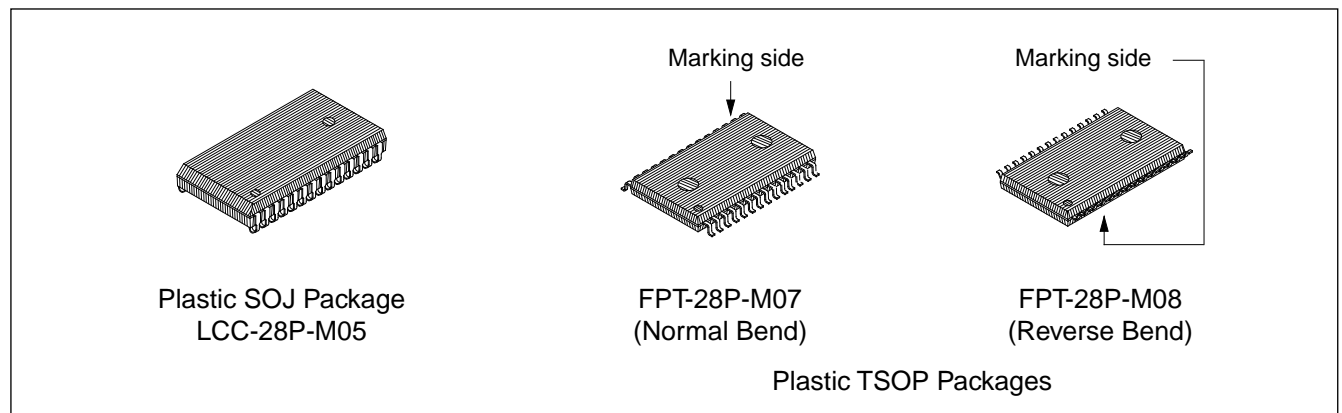
1

MB81V4800S-60/MB81V4800S-70

■ PRODUCT LINE & FEATURES

Parameter		MB81V4800S-60	MB81V4800S-70
$\overline{\text{RAS}}$ Access Time		60 ns max.	70 ns max.
$\overline{\text{CAS}}$ Access Time		20 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.
Random Cycle Time		110 ns max.	125 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Low Power Dissipation	Operating current	234 mW max.	209 mW max.
	Standby current	7.2 mW max. (LVTTL level),3.6 mW max. (CMOS level)	

- Low V$_{CC}$ operating
- 524,288 words × 8 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are LVTTL comaptible
- 1024 refresh cycles every 16.4 ms
- 10 rows × 9 columns, addressing scheme
- Early Write or $\overline{\text{OE}}$ controlled Write capability
- $\overline{\text{RAS}}$ only $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, or Hidden Refresh
- Self refresh function
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

■ PACKAGE

Marking side

Marking side

Plastic SOJ Package
LCC-28P-M05

FPT-28P-M07
(Normal Bend)

FPT-28P-M08
(Reverse Bend)

Plastic TSOP Packages

Package and Ordering Information

– 28-pin plastic (400 mil) SOJ, order as MB81V4800S-××PJ

– 28-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB81V4800S-××PFTN

– 28-pin plastic (400 mil) TSOP-II with reverse bend leads, order as MB81V4800S-××PFTR
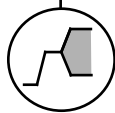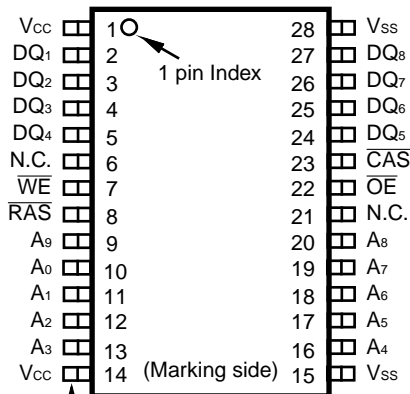
MB81V4800S-60/MB81V4800S-70
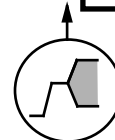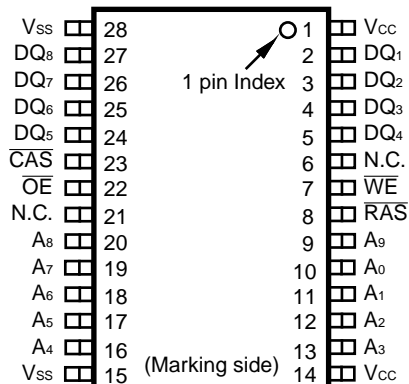
■ CAPACITANCE

($T_A = 25°C$, f = 1 MHz)

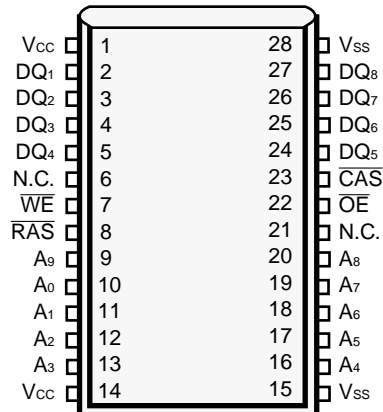| Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	7	pF
Input/Output Capacitance, DQ_1 to DQ_8	C_{DQ}	—	7	pF

■ PIN ASSIGNMENTS AND DESCRIPTIONS

28-Pin TSOP:
(TOP VIEW)
<Normal Bend: FPT-28P-M07>

V_{CC}	1	28 V_{SS}
DQ_1	2	27 DQ_8
DQ_2	3	26 DQ_7
DQ_3	4	25 DQ_6
DQ_4	5	24 DQ_5
N.C.	6	23 $\overline{CAS}$
$\overline{WE}$	7	22 $\overline{OE}$
$\overline{RAS}$	8	21 N.C.
A_9	9	20 A_8
A_0	10	19 A_7
A_1	11	18 A_6
A_2	12	17 A_5
A_3	13	16 A_4
V_{CC}	14 (Marking side)	15 V_{SS}

1 pin Index

28-Pin SOJ:
(TOP VIEW)
<LCC-28P-M05>

V_{CC}	1	28 V_{SS}
DQ_1	2	27 DQ_8
DQ_2	3	26 DQ_7
DQ_3	4	25 DQ_6
DQ_4	5	24 DQ_5
N.C.	6	23 $\overline{CAS}$
$\overline{WE}$	7	22 $\overline{OE}$
$\overline{RAS}$	8	21 N.C.
A_9	9	20 A_8
A_0	10	19 A_7
A_1	11	18 A_6
A_2	12	17 A_5
A_3	13	16 A_4
V_{CC}	14	15 V_{SS}

(TOP VIEW)
<Reverse Bend : FPT-28P-M08>

V_{SS}	28	1 V_{CC}
DQ_8	27	2 DQ_1
DQ_7	26	3 DQ_2
DQ_6	25	4 DQ_3
DQ_5	24	5 DQ_4
$\overline{CAS}$	23	6 N.C.
$\overline{OE}$	22	7 $\overline{WE}$
N.C.	21	8 $\overline{RAS}$
A_8	20	9 A_9
A_7	19	10 A_0
A_6	18	11 A_1
A_5	17	12 A_2
A_4	16 (Marking side)	13 A_3
V_{SS}	15	14 V_{CC}

1 pin Index

Designator	Function
A_0 to A_9	Address inputs row : A_0 to A_9 column : A_0 to A_8 refresh : A_0 to A_9
$\overline{RAS}$	Row address strobe.
$\overline{CAS}$	Column address strobe.
$\overline{WE}$	Write Enable.
$\overline{OE}$	Output enable.
DQ_1 to DQ_8	Data Input/ Output
V_{CC}	+3.3 volt power supply.
V_{SS}	Circuit ground.

3

MB81V4800S-60/MB81V4800S-70

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage		$\boxed{1}$	V_{CC}	3.0	3.3	3.6	V	0°C to +70°C
			V_{SS}	0	0	0		
Input High Voltage, all inputs		$\boxed{1}$	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage, all inputs(*)		$\boxed{1}$	V_{IL}	−0.3	—	0.8	V	
Input Low Voltage, DQ(*)		$\boxed{1}$	V_{ILD}	−0.3	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Nineteen input bits are required to decode any eight of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 5. First, ten row address bits are input on pins A_0-through-A_9 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input on pins A_0-through-A_8 and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are the flow-through type; thus, address information appearing after t_{RAH} (min.) + t_T is automatically treated as the column address to start select operation of the column decode. Therefore, to have correct data within t_{RAC}, the column address should be input within t_{RAD} (max.). If $t_{RAD} > t_{RAD}$ (max.), the access time is the later one of either t_{AA} or t_{CAS}.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data are ignored. When an early write cycle is executed, the output buffers stay in a high-impedance state during the cycle.

DATA INPUT

Input data are written into memory in either of three basic ways—the early write cycle, the $\overline{OE}$ (delayed) write cycle, and the read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In the early write cycle, the input data (DQ_1-DQ_8) are strobed by $\overline{CAS}$ and the setup/hold times are referenced to falling edge of $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In the delayed write or read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the falling edge of $\overline{WE}$. Since this device is an I/O common type, when the delayed write or read-modified-write is executed, I/O data have to be controlled by $\overline{OE}$.

DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max.) is satisfied.

t_{CAC} : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max.).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max.).

t_{OEA} : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

4

MB81V4800S-60/MB81V4800S-70

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512×8-bits can be accessed. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

MB81V4800S-60/MB81V4800S-70

■ DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)   Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output high voltage	1	V_{OH}	$I_{OH} = -2.0$ mA	2.4	—	—	V
Output low voltage	1	V_{OL}	$I_{OL} = +2.0$ mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0\ V \leq V_{IN} \leq 3.6\ V$; $3.0\ V \leq V_{CC} \leq 3.6\ V$; $V_{SS} = 0\ V$; All other pins not under test = 0 V	−10	—	10	μA
Output leakage current		$I_{DQ(L)}$	$0\ V \leq V_{OUT} \leq 3.6\ V$; Data out disabled	−10	—	10	
Operating current (Average Power supply current) 2	MB81V4800S-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{RC} = $ min.	—	—	65	mA
	MB81V4800S-70					58	
Standby current (Power supply current)	LVTTL level	I_{CC2}	$\overline{RAS} = \overline{CAS} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\ V$			1.0	
Refresh current #1 (Average power supply current) 2	MB81V4800S-60	I_{CC3}	$\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; $t_{RC} = $ min.	—	—	65	mA
	MB81V4800S-70					58	
Fast Page Mode current 2	MB81V4800S-60	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{PC} = $ min.	—	—	65	mA
	MB81V4800S-70					58	
Refresh current #2 (Average power supply current) 2	MB81V4800S-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC} = $ min.	—	—	65	mA
	MB81V4800S-70					58	
Refresh current #3 (Average power supply current)	2	I_{CC9}	$\overline{RAS} = V_{IL}$, $\overline{CAS} = V_{IL}$ Self refresh; $t_{RASS} = $ min.	—	—	1000	μA

MB81V4800S-60/MB81V4800S-70

■ AC CHARACTERISTICS
(At recommended operating conditions unless otherwise noted.)   Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4800S-60		MB81V4800S-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	170	—	ns
4	Access Time from $\overline{RAS}$	6, 9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	7, 9	t_{CAC}	—	20	—	20	ns
6	Column Address Access Time	8, 9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_T	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11, 12	t_{RCD}	20	40	20	50	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	10000	20	10000	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	ns
29	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	ns

(Continued)

MB81V4800S-60/MB81V4800S-70
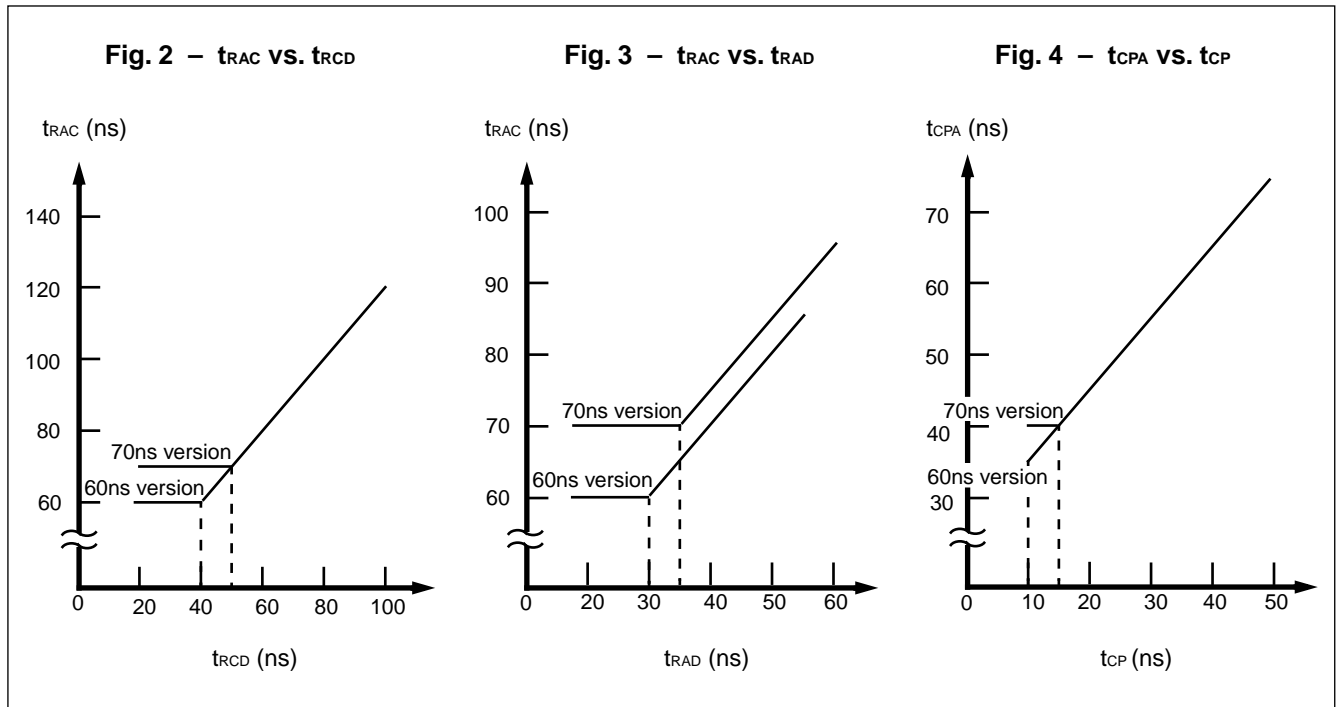
■ AC CHARACTERISTICS (Continued)
(At recommended operating conditions unless otherwise noted.)   Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4800S-60		MB81V4800S-70		Unit
				Min.	Max.	Min.	Max.	
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	ns
34	DIN Set Up Time		t_{DS}	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	10	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	85	—	95	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	40	—	40	—	ns
38	Column Address to $\overline{WE}$ Delay Time		t_{AWD}	55	—	60	—	ns
39	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	10	—	10	—	ns
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	ns
42	Access Time from $\overline{OE}$	9	t_{OEA}	—	20	—	20	ns
43	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	15	ns
44	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
45	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	ns
46	$\overline{OE}$ to Data in Delay Time		t_{OED}	15	—	15	—	ns
47	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	ns
48	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	ns
49	Column Address Hold Time from $\overline{RAS}$		t_{CDD}	15	—	15	—	ns
50	Write Command Hold Time from $\overline{RAS}$		t_{AR}	32	—	32	—	ns
51	DIN Hold Time Referenced to $\overline{RAS}$		t_{WCR}	30	—	30	—	ns
52	$\overline{CAS}$ to Data in Delay Time		t_{DHR}	30	—	30	—	ns
60	Fast Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	60	200000	70	200000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	90	—	ns
63	Access Time from $\overline{CAS}$ Precharge	9, 18	t_{CPA}	—	35	—	40	ns
64	Fast Page Mode $\overline{CAS}$ Pulse width		t_{CP}	10	—	10	—	ns
65	Fast Page Mode $\overline{RAS}$ Hold Time from CAS Precharge		t_{RHCP}	35	—	40	—	ns
66	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	55	—	60	—	ns

Notes: 1. Referenced to V_{SS}. To all V_{CC} (V_{SS}) pins, the same supply voltage should be applied.

2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
    I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, $V_{IL} > -0.5$ V.
    I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
    I_{CC4} is specified at one time of address change during one Page cycle.

3. An Initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

4. AC characteristics assume $t_T = 5$ ns.

5. Input voltage levels are 0 V and 3.0 V, and input reference levels are V_{IH} (min.) and V_{IL} (max.) for measuring timing of input signals. Also, the transition time (t_T) is measured between V_{IH} (min.) and V_{IL} (max.).
    The output reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.

6. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.

7. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

8. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

9. Measured with a load equivalent to one TTL loads and 100 pF.

10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.

11. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

12. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).

13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min.) the data output pin will remain High-Z state through entire cycle.

16. Assumes that $t_{WCS} < t_{WCS}$ (min.).

17. Either t_{DZC} or t_{DZO} must be satisfied.

18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max.).

19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

MB81V4800S-60/MB81V4800S-70

Fig. 2 − t_{RAC} vs. t_{RCD}

t_{RAC} (ns)

140 —
120 —
100 —
80 —
70ns version
60ns version
60 —

0   20   40   60   80   100

t_{RCD} (ns)

Fig. 3 − t_{RAC} vs. t_{RAD}

t_{RAC} (ns)

100 —
90 —
80 —
70ns version
70 —
60ns version
60 —

0   20   30   40   50   60

t_{RAD} (ns)

Fig. 4 − t_{CPA} vs. t_{CP}

t_{CPA} (ns)

70 —
60 —
50 —
70ns version
40 —
60ns version
30 —

0   10   20   30   40   50

t_{CP} (ns)

■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Col-umn	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min.)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min.)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes*	
$\overline{RAS}$-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.)
Hidden Refresh Cycle	H→L	L	H	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

MB81V4800S-60/MB81V4800S-70

Fig. 5 – READ CYCLE
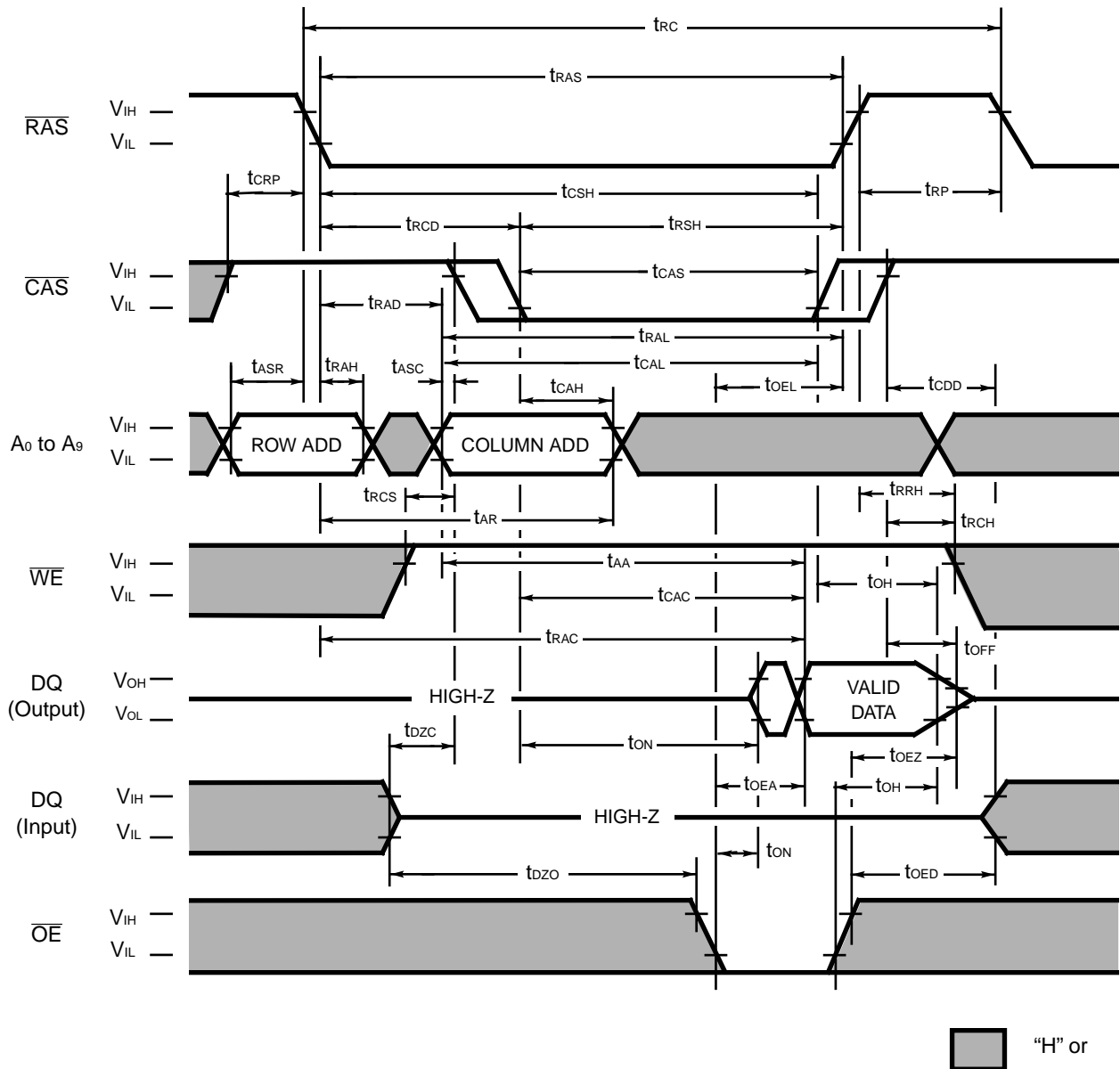
DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}(t_{RAC})$, $\overline{CAS}$ (t_{CAC}), $\overline{OE}$ (t_{OEA}) or column addresses (t_{AA}) under the following conditions:
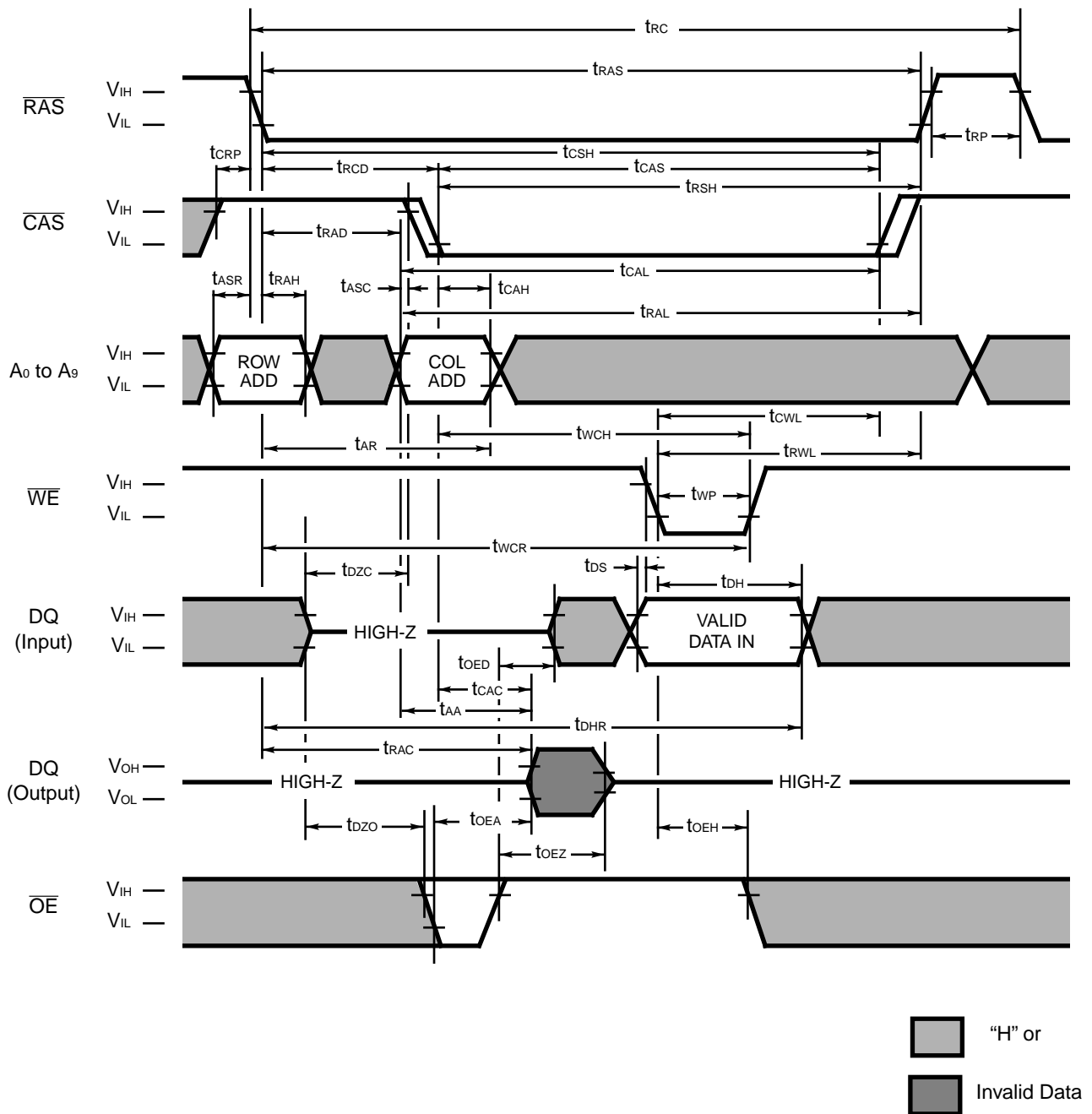
If $t_{RCD} > t_{RCD}$ (max.), access time = t_{CAC}.

If $t_{RAD} > t_{RAD}$ (max.), access time = t_{AA}.

If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

11

MB81V4800S-60/MB81V4800S-70

Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways - early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory.
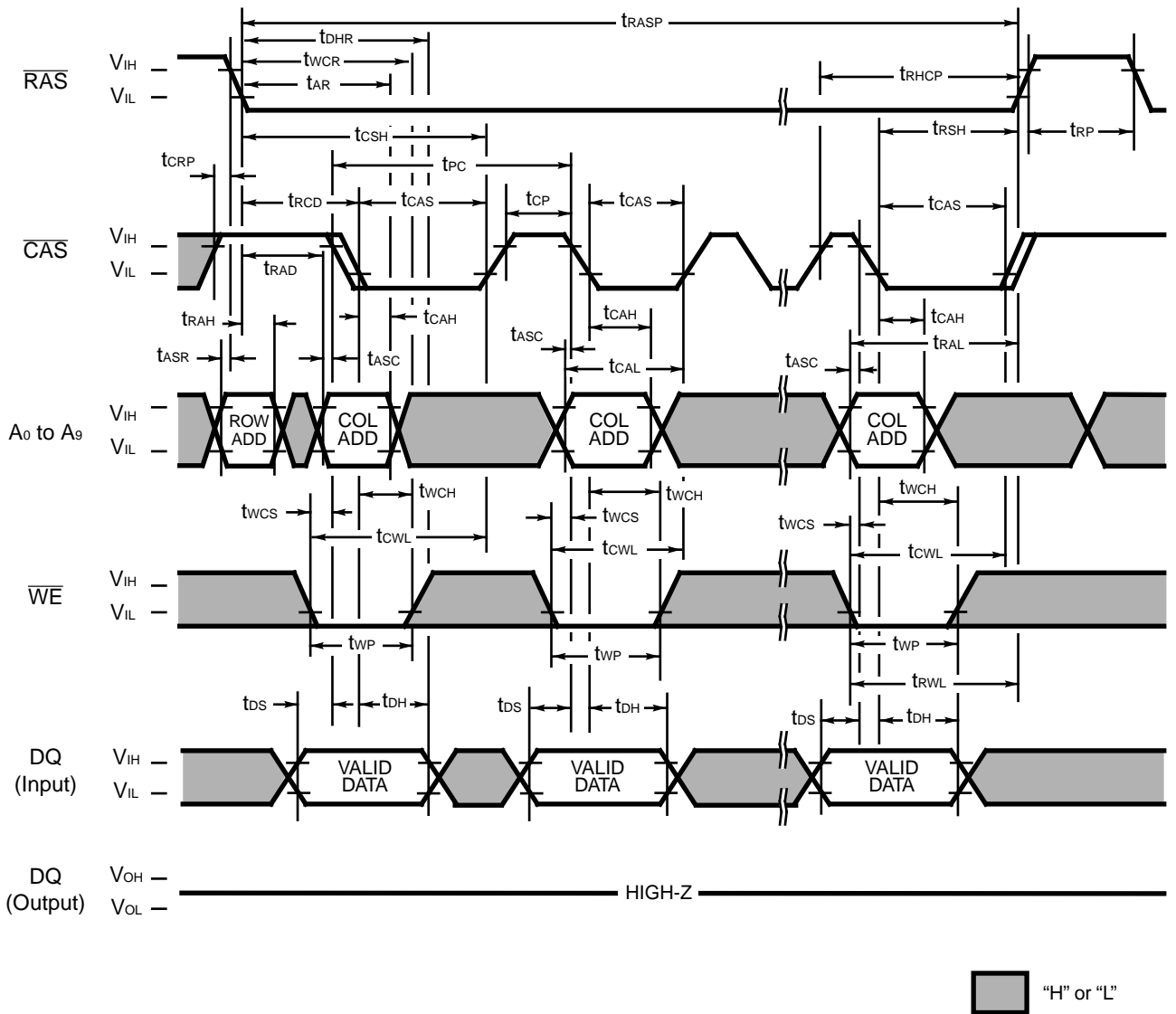
12

MB81V4800S-60/MB81V4800S-70

Fig. 7 – $\overline{OE}$ (DELAYED WRITE) CYCLE

DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

13

MB81V4800S-60/MB81V4800S-70

Fig. 8 – READ-MODIFY-WRITE CYCLE

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

14

MB81V4800S-60/MB81V4800S-70

Fig. 9 – FAST PAGE MODE READ CYCLE

DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.
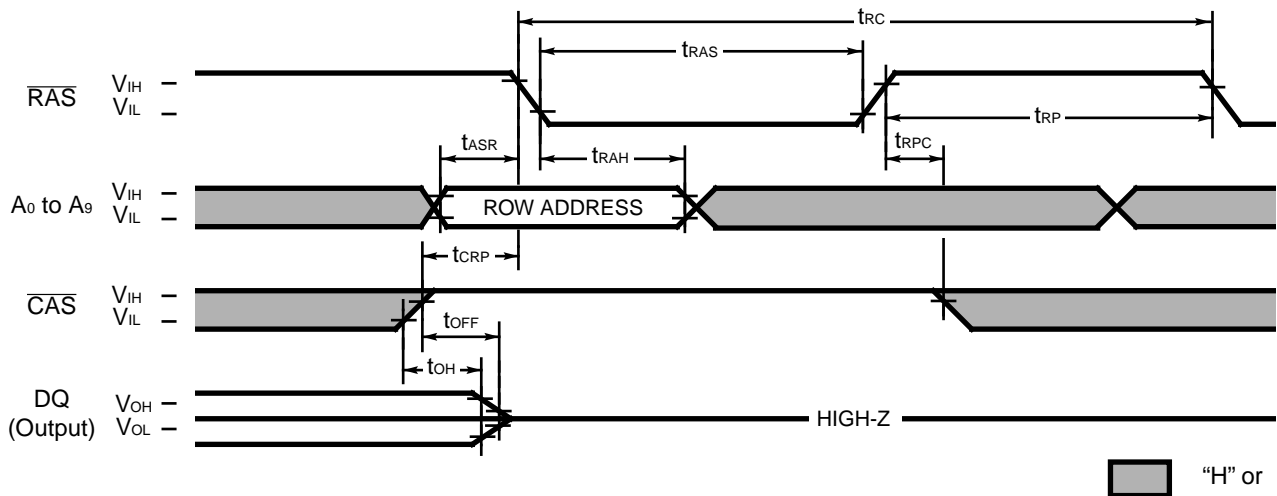
MB81V4800S-60/MB81V4800S-70

Fig. 10 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")

DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

MB81V4800S-60/MB81V4800S-70

Fig. 11 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

| | "H" or "L" |
| | Invalid Data |

DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

17

MB81V4800S-60/MB81V4800S-70

Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE

DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

MB81V4800S-60/MB81V4800S-70

Fig. 13 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE} = \overline{OE}$ = "H" or "L")

DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1024 row addresses every 16.4-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE} = \overline{OE}$ = "H" or "L")
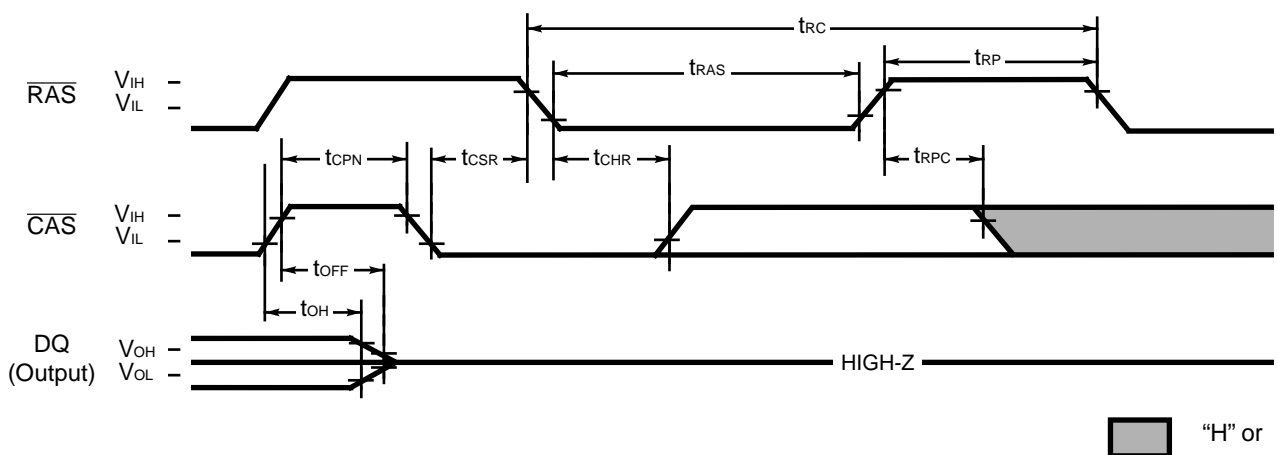
DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

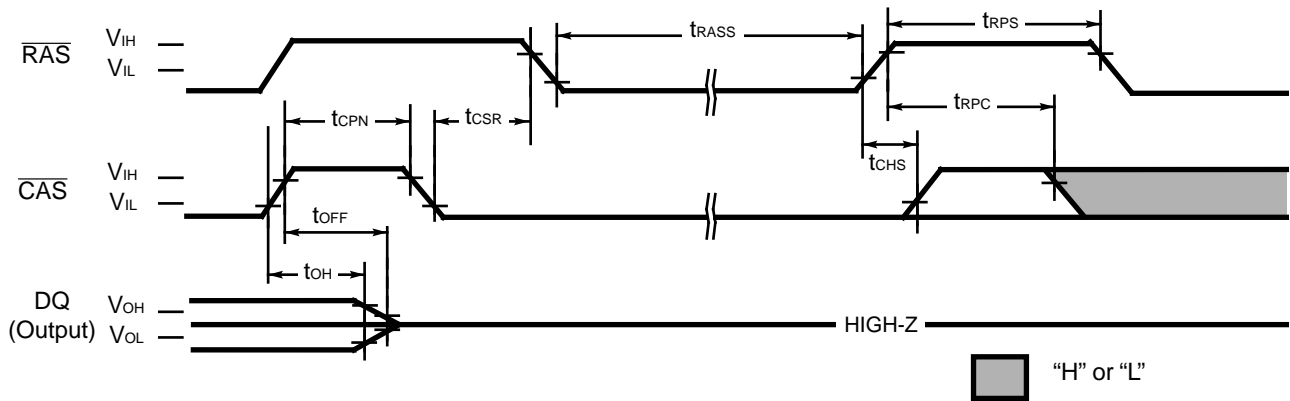# MB81V4800S-60/MB81V4800S-70

Fig. 15 – HIDDEN REFRESH CYCLE

"H" or
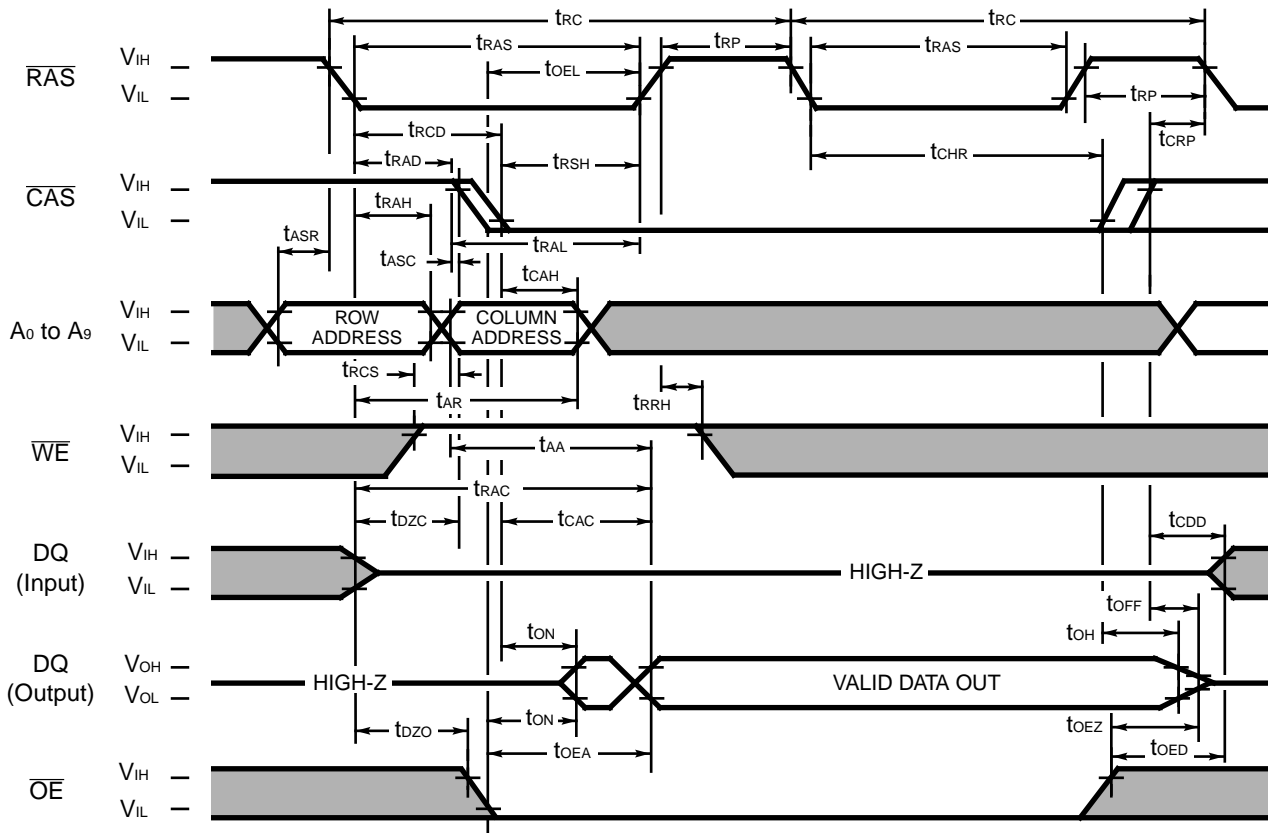
DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{CAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

MB81V4800S-60/MB81V4800S-70

Fig. 16 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_9 are defined by the on-chip refresh counter.
Column Address: Bits A_0 through A_8 are defined by latching levels on A_0-A_8 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows;
1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4800S-60		MB81V4800S-70		Unit
			Min.	Max.	Min.	Max.	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	55	—	55	ns
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	ns
92	$\overline{CAS}$ to WE Delay Time	t_{FCWD}	80	—	80	—	ns
93	$\overline{CAS}$ Pulse width	t_{FCAS}	55	—	55	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	55	—	55	—	ns
95	$\overline{CAS}$ Hold Time	t_{FCSH}	85	—	85	—	ns

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

MB81V4800S-60/MB81V4800S-70

Fig. 17 – SELF REFRESH CYCLE (A$_0$ - A$_9$ = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4800S-60		MB81V4800S-70		Unit
			Min.	Max.	Min.	Max.	
100	$\overline{RAS}$ Pulse Width	t_{RASS}	100	—	100	—	ns
101	$\overline{RAS}$ Precharge Time	t_{RPS}	110	—	125	—	ns
102	$\overline{CAS}$ Hold Time	t_{CHS}	−50	—	−50	—	ns

Note: Assumes Self refresh cycles only.

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter. If /CAS goes to "L" before /RAS goes to "L" (CBR) and the condition of /CAS "L" and /RAS "L" is kept for term of tRASS (more than 100 μs), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during "/RAS = L" and "/CAS = L".
And exit from self refresh cycle is performed by toggling of /RAS and /CAS to "H" with specifying tCHS min.

Restruction for Self refresh operation;
For self refresh operation, the notice below must be considered.

1) In the case that distribut CBR refresh are operated in read/write cycles
   Self refresh cycles can be executed without special rule if 1024 cycles of distribut CBR refresh are executed within tREF max..
2) In the case that burst CBR refresh or /RAS only refresh are operated in read/write cycles
   1024 times of burst CBR refresh or 1024 times of burst /RAS only refresh must be executed before and after Self refresh cycles.
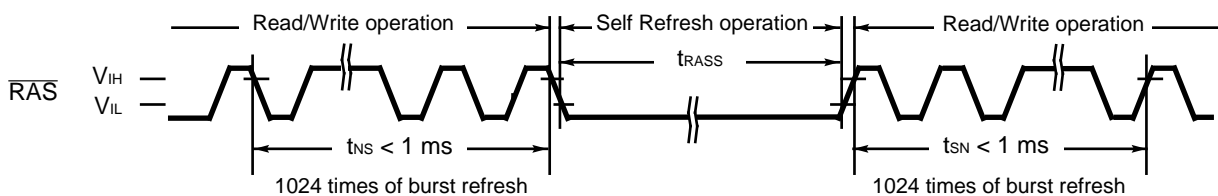
MB81V4800S-60/MB81V4800S-70

■ PACKAGE DIMENSIONS

(Suffix: -PJ)

28 pin, Plastic SOJ
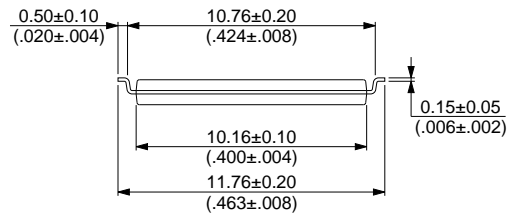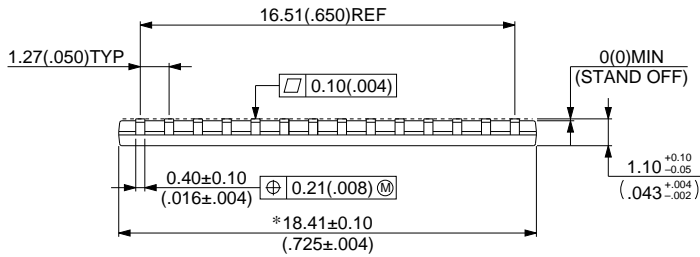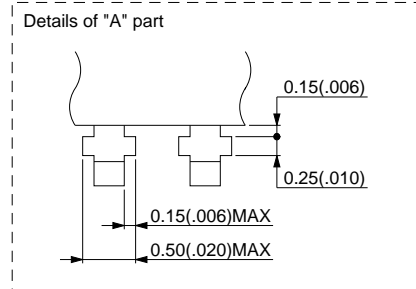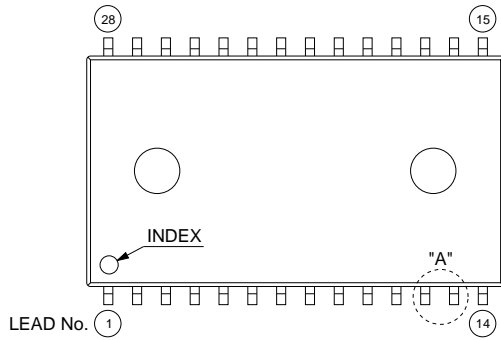(LCC-28P-M05)

Dimensions in mm(inches).

© 1995 FUJITSU LIMITED C28055S-4C-1
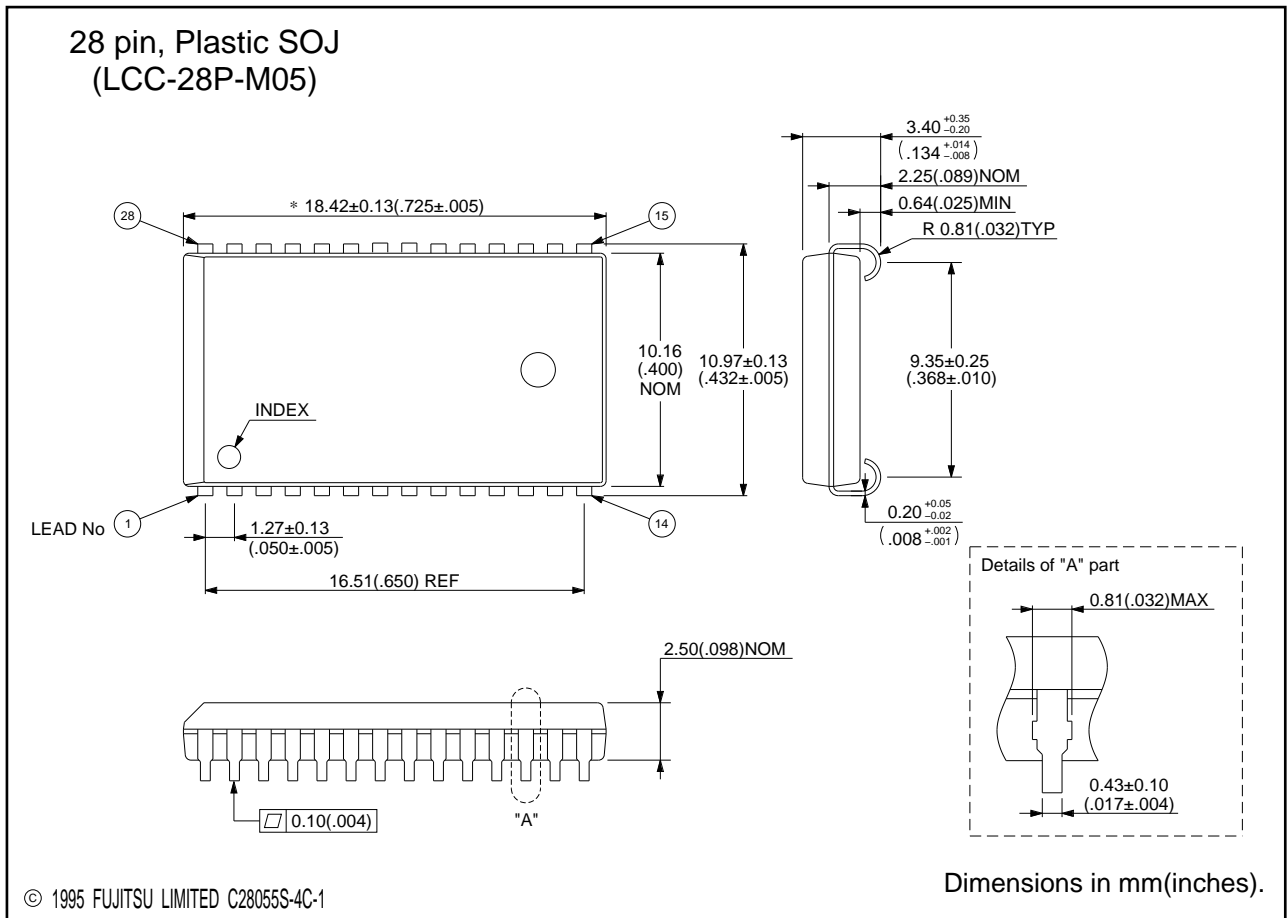
MB81V4800S-60/MB81V4800S-70

■ **PACKAGE DIMENSIONS** (Continued)

(Suffix: -PFTN)

28 pin, Plastic TSOP(II)
(FPT-28P-M07)
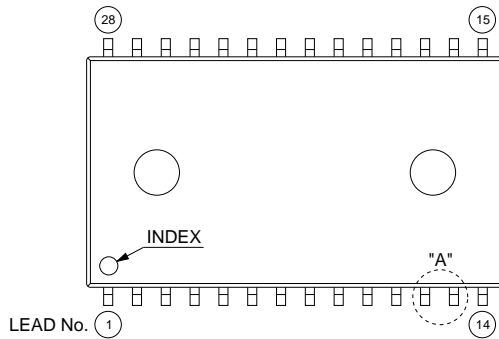
Details of "A" part
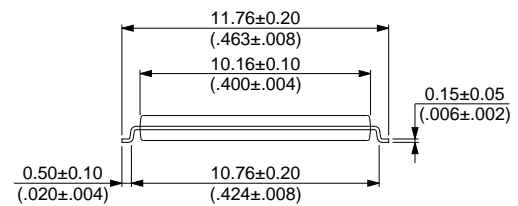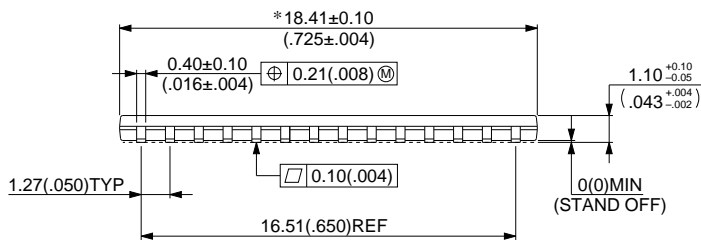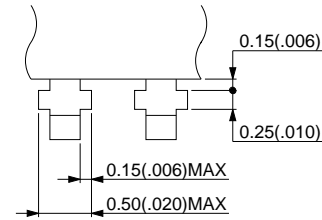
0.15(.006)

0.25(.010)

0.15(.006)MAX

0.50(.020)MAX

INDEX

LEAD No. ①   ⑭

*18.41±0.10
(.725±.004)

0.40±0.10   ⊕ 0.21(.008) Ⓜ
(.016±.004)

1.10 $^{+0.10}_{-0.05}$
(.043 $^{+.004}_{-.002}$)

▢ 0.10(.004)

1.27(.050)TYP

0(0)MIN
(STAND OFF)

16.51(.650)REF

11.76±0.20
(.463±.008)

10.16±0.10
(.400±.004)

0.15±0.05
(.006±.002)

0.50±0.10
(.020±.004)

10.76±0.20
(.424±.008)

Dimensions in mm(inches).

© 1994 FUJITSU LIMITED F28031S-1C-2

24

■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

28 pin, Plastic TSOP(II)
(FPT-28P-M08)

Details of "A" part

0.15(.006)

0.25(.010)

0.15(.006)MAX

0.50(.020)MAX

INDEX

"A"

LEAD No. ①   ⑭

16.51(.650)REF

1.27(.050)TYP

0.10(.004)

0(0)MIN
(STAND OFF)

0.50±0.10
(.020±.004)

10.76±0.20
(.424±.008)

0.40±0.10
(.016±.004)   ⊕ 0.21(.008) Ⓜ

1.10 $^{+0.10}_{-0.05}$
(.043 $^{+.004}_{-.002}$)

0.15±0.05
(.006±.002)

*18.41±0.10
(.725±.004)

10.16±0.10
(.400±.004)

11.76±0.20
(.463±.008)

Dimensions in mm(inches).

© 1994 FUJITSU LIMITED F28032S-1C-2

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

F9703
© FUJITSU LIMITED Printed in Japan